IN THE SPECIFICATION:

Paragraph at page 10, line 8:

A first pattern (or, upper pattern) 8 is formed at the surface of the wiring substrate 4 on which the semiconductor chip 2 is placed, while a second pattern (or, lower pattern) 10 is formed at a surface of the wiring substrate 4 opposite the first pattern 8. The first wiring pattern 8 and the second wiring pattern 10 are connected to each other via through holes 12 which pass through the wiring substrate 4.

Paragraph at page 14, line 9:

The sealing resin layer 6 is formed on the circuit substrate and has a thickness of about 400 μm. Fig. 6 shows that the resin layer 6 is formed in a first region on the upper surface of the substrate 4. The first region, which includes the first (upper) metal pattern 8, is shown inside a second region on the upper surface of the substrate 4. The second region includes the registration marks L, and forms a border around the first region in Fig. 6. The boundary between the first region and the second region is the inner rectangle in Fig. 6. The registration marks L are formed at two corners of the inner rectangle, which covers the coinciding rectangular array of semiconductor chips 2 shown in Fig. 5.

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